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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

TAKENO

Group Art Unit:

Serial No.: New Application

Examiner:

Filed: September 24, 2001

Docket No. P107242-00024

For: MANUFACTURING PROCESS FOR SILICON EPITAXIAL WAFER

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

September 24, 2001

Sir:

Prior to calculation of the filing fee and prior to the examination of this application, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the title to read -- MANUFACTURING PROCESS FOR SILICON EPITAXIAL WAFER --.

IN THE CLAIMS:

Please cancel original claims 1 through 5 and add the following claims:

-- 6. (Added) A manufacturing process for a silicon epitaxial wafer comprising the steps of:

forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from $4 \times 10^{17}/cm^3$ to $10 \times 10^{17}/cm^3$ at a temperature of 1000° C or higher to obtain a silicon epitaxial wafer; and

applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C.

7. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein the interstitial oxygen concentration is in a range of from $6 \times 10^{17}/cm^3$ to $10 \times 10^{17}/cm^3$.

8. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein the heat treatment temperature is in a range of from 500° C to 700° C.

9. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein the heat treatment temperature is in a range of from 500° C to 700° C.

10. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

11. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

12. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 8, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

13. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 9, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

14. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

15. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

16. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 8, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

17. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 9, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

18. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 10, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

19. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 11, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

20. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 12, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

21. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 13, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony. --

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REMARKS

The above amendments to the claims have been made to correct the multiple dependency of the claims and to put the application in better condition for examination. No new matter has been added.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2300.

Respectfully submitted,

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